# Refine Search

**Search Results -**

| Terms | Documents |
|---|---|
| L11 same L3 | 0 |

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**Search:** L13

Refine Search | Recall Text | Clear | Interrupt

## Search History

**DATE: Tuesday, May 23, 2006** Printable Copy Create Case

| Set Name side by side | Query | Hit Count | Set Name result set |
|---|---|---|---|
| *DB=USPT,USOC,EPAB,JPAB,DWPI,TDBD; PLUR=YES; OP=OR* | | | |
| L13 | L11 same l3 | 0 | L13 |
| L12 | L11 and l6 | 0 | L12 |
| L11 | L1 same l2 | 30 | L11 |
| L10 | l1 same l6 | 0 | L10 |
| L9 | L6 same l3 | 6 | L9 |
| L8 | L7 same l6 | 0 | L8 |
| L7 | L4 same l5 | 229 | L7 |
| L6 | reduc$ adj1 susceptibility | 5906 | L6 |
| L5 | rout$ | 671565 | L5 |
| L4 | unrout$ | 267 | L4 |
| L3 | pld or (programmable adj1 logic) | 34289 | L3 |
| L2 | seu | 5218 | L2 |
| L1 | single-event adj1 upset | 67 | L1 |

First Hit Fwd Refs Previous Doc Next Doc Go to Doc#

Generate Collection Print

L9: Entry 3 of 6 File: USPT Sep 9, 2003

DOCUMENT-IDENTIFIER: US 6617912 B1
TITLE: Pass gate multiplexer circuit with reduced susceptibility to single event upsets

Abstract Text (1):
A multiplexer circuits for programmable logic devices (PLDs) reduced susceptibility to single event upsets. The pass gate multiplexer circuit has N input circuits having pass gate and N memory cells controlling the pass gates. Each path between an input terminal and the output node includes two pass gates controlled by different memory cells. Therefore, a single event upset that inadvertently enables a pass gate can only short two input terminals when the other,pass gate in the affected input path is also enabled by its associated memory cell. Therefore, the multiplexer circuit with two pass gates in each input path reduces the susceptibility to single event upsets by a factor of (N-4)/N.

Brief Summary Text (14):
Thus, the multiplexer structure of FIG. 1 is susceptible to single event upsets. Further, as operating voltages diminish, static RAM cells become more susceptible to changes in state caused by single event upsets. To reduce manufacturing costs, PLD manufacturers are aggressively reducing device sizes in their PLDs. These smaller devices often operate at lower voltages. Therefore, the effects of single event upsets are becoming more important over time. It is desirable to provide PLD circuits with reduced susceptibility to single event upsets, particularly commonly-used circuits such as multiplexing circuits.

Brief Summary Text (16):
The invention provides multiplexer circuits for programmable logic devices (PLDs) that have reduced susceptibility to single event upsets. A standard pass gate multiplexer circuit having N pass gates and N memory cells controlling the pass gates is modified to include additional N pass gates, one on each input path. Thus, each path between an input terminal and the output node includes two pass gates controlled by different memory cells.

Previous Doc Next Doc Go to Doc#

L9: Entry 2 of 6 File: USPT Dec 30, 2003

DOCUMENT-IDENTIFIER: US 6671202 B1
TITLE: Programmable circuit structures with reduced susceptibility to single event upsets

Brief Summary Text (17):
Therefore, the effects of single event upsets are becoming more important over time. Hence, it is desirable to provide PLD circuits with reduced susceptibility to single event upsets.

Brief Summary Text (19):
The invention provides circuit structures for programmable logic devices (PLDS) that have reduced susceptibility to single event upsets. A circuit structure according to the invention includes a programmable circuit controlled by memory cells. The programmable circuit is designed such that at most one of the memory cells in a group of the memory cells has an enable value at any given time. According to the invention, the memory cells are coupled together such that if any one memory cell in the group is at an enable value (e.g., high), then all other memory cells in the same group are forced to a disable value (e.g., low).

Brief Summary Text (26):
According to a third embodiment of the invention, a system having reduced susceptibility to single event upsets includes a plurality of programmable logic circuits, a plurality of interconnect lines programmably coupling the programmable logic circuits to each other, and a group of memory cells coupled to control terminals of at least one of the programmable circuits. Of the control terminals, at most one provides an enable value at any given time. Each memory cell drives an initialization input terminal of each other memory cell in the group of memory cells.

Brief Summary Text (28):
According to a fourth embodiment of the invention, a system having reduced susceptibility to single event upsets includes a plurality of programmable logic circuits, an interconnect structure that includes a plurality of interconnect circuits, the interconnect structure programmably coupling the programmable logic circuits to each other, and a group of memory cells coupled to control terminals of at least one of the interconnect circuits. Of the control terminals, at most one provides an enable value at any given time. Each memory cell drives an initialization input terminal of each other memory cell in the group of memory cells.

CLAIMS:

21. A system having reduced susceptibility to single event upsets, the system comprising: a plurality of programmable logic circuits, at least one of the programmable logic circuits having a plurality of control terminals, wherein at most one of the control terminals provides an enable value at any given time; a plurality of interconnect lines programmably coupling the programmable logic circuits to each other; and a first group of two or more memory cells, each memory cell having at least one initialization input terminal and further having an output terminal coupled to a control terminal of the at least one programmable circuit,

each memory cell in the first group driving an initialization input terminal of each other memory cell in the first group.

27. A system having reduced susceptibility to single event upsets, the system comprising: a plurality of programmable logic circuits; an interconnect structure programmably coupling the programmable logic circuits to each other, the interconnect structure comprising a plurality of interconnect circuits, at least one of the interconnect circuits having a plurality of control terminals wherein at most one of the control terminals provides at enable value at any given time; and a first group of two or more memory cells, each memory cell having at least one initialization input terminal and further having an output terminal coupled to a control terminal of the at least one interconnect circuit, each memory cell in the first group driving an initialization input terminal of each other memory cell in the first group.

Previous Doc Next Doc Go to Doc#